Latent Damage from Single-Event Latchup

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Abstract:

Permanent damage effects are studied for several types of CMOS circuits that are sensitive to single-event latchup. The emphasis is placed on latent damage effects, where devices remained functional despite significant structural damage to their interconnects. This type of damage was observed during latchup testing with both laser pulses and heavy ions. Microscopic examination of the damaged regions after latchup testing revealed small metallic spheres and cracked, voided interconnects. A full description of the characteristic physical signatures of latent damage is included, along with key parameters of these types of events.

A physical interpretation of latchup-induced structural damage is presented. Analysis and diagnostic studies of damaged devices with scanning electron microscopy indicate that the high current densities involved during latchup cause melting and expansion of interconnect metal and subsequent eruption from the encasing insulator material. Latent damage was found to occur most often in the top level of metallization, which is attributed to its distance from the silicon substrate heat sink relative to lower levels of metal. Data to date on the current densities and event durations involved for non-destructive latchup events correspond to conditions for failure indicated by previous studies. An explanation of why some structurally damaging latchup events are non-catastrophic is presented.

Because this type of structural damage is permanent, it raises a concern about vulnerability to future device failure. Latchup circumvention efforts should take this type of damage into account, especially since it often occurs over very short time periods and is difficult to observe. Next generation devices are expected to contain smaller interconnects and more levels of metallization, and therefore may exhibit a higher rate of this type of latent damage.

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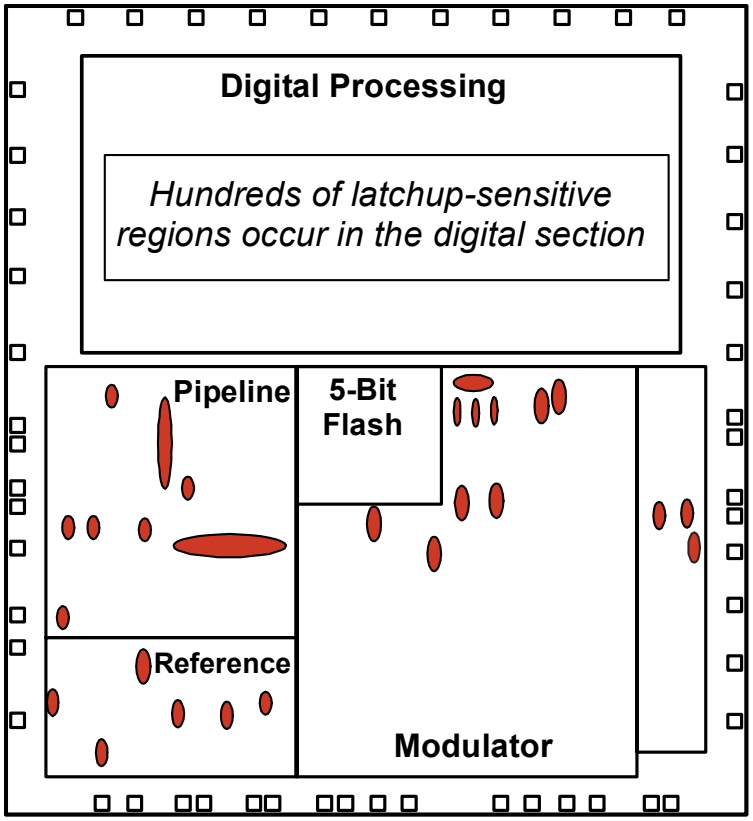
Outline

- Initial Interest & Observations
- Data
- Analysis
- Conclusions

Initial Interest: *Catastrophic* SEL

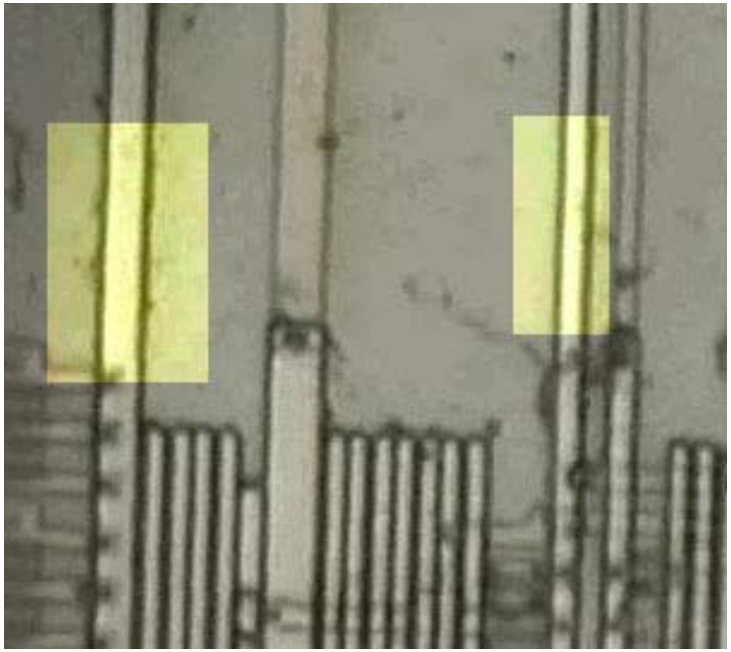
- How are SEL failures related to device properties?
- AD9260 failed from latchup during heavy ion testing
- Laser-induced SEL testing at the Aerospace Corp.
  - induce latchup with laser pulses
  - observe latchup equilibrium currents
  - monitor device functionality
  - observe irradiated area on the die through CCD camera/video monitor

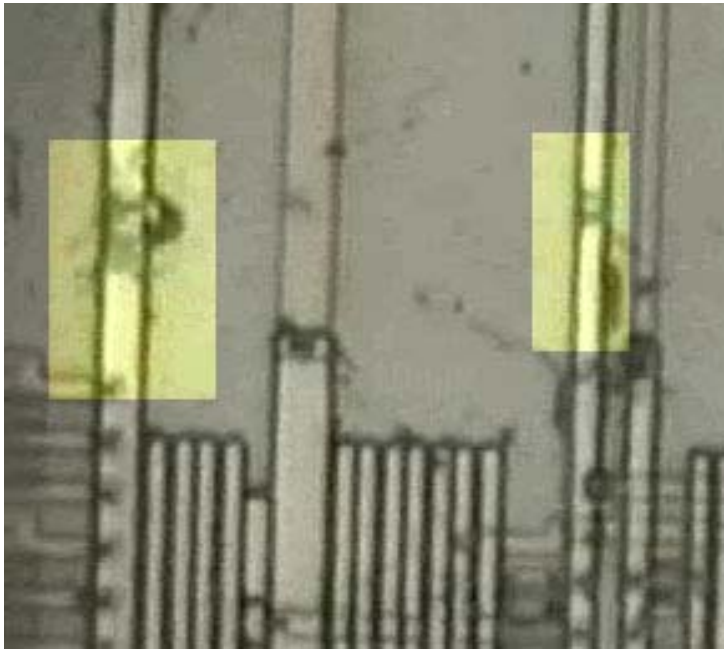
Initial Interest: Identification of Latchup-Sensitive Regions



28 latchup-sensitive regions with distinct geometries and equilibrium currents were located in analog section of the AD9260

An Unexpected Observation





- A structurally damaging SEL was observed
- The DUT was still *functional* after holding 200mA for 1ms
- Reproducible experiment: 50% functional, 50% destroyed

Data: CMOS Devices Studied for SEL-Induced Structural Damage

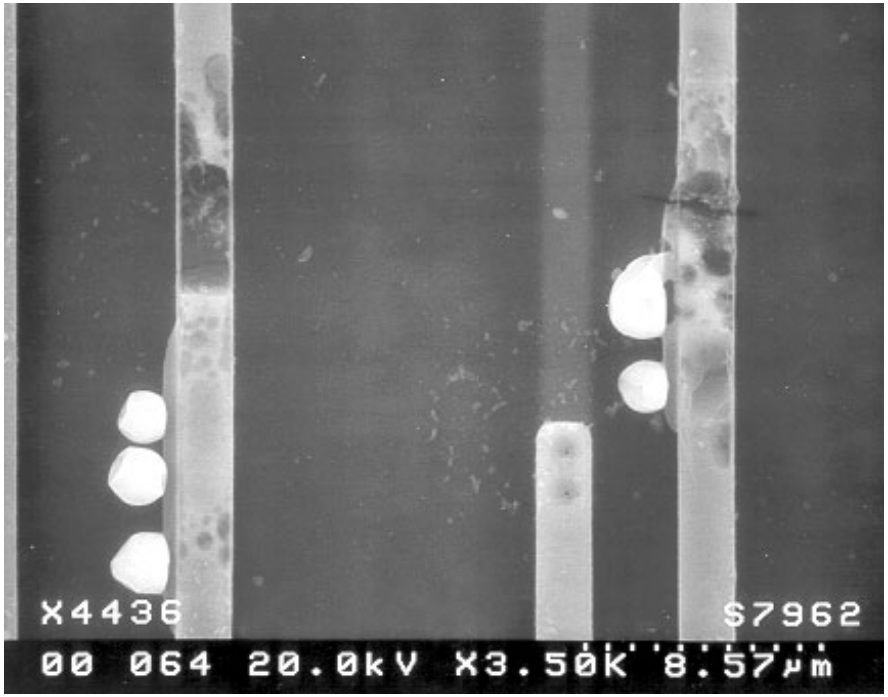
CMOS Device	Device Type	Manufacturer	Latent Damage
AD9260	ADC	Analog Devices	Yes
AD9240	ADC	Analog Devices	No
ADC10321	ADC	NSC	Yes
CAR/CPPX1T-A7BR	Oscillator	Cardinal/Cypress Hybrid	Yes
LTC1799	Oscillator	Linear Technology	No
ADSP2100	DSP	Analog Devices	No

Data: Methods/Diagnostic Approaches

- Testing with Cf^{252}
  - SEL equilibrium current & DUT functionality monitored
  - DUT removed from chamber after SEL events
- Optical microscopy
  - Die is scanned for potential damage sites
  - Often difficult due to the complexity of many CMOS circuits
- Scanning Electron Microscopy (SEM)
  - Better resolution
  - Energy Dispersive Spectroscopy (EDS) reveals properties of damage site

Data: Latent Damage Signatures

- Aluminum spheres
- Cracking of insulator material (silicon nitride/silicon dioxide)
- Significant voiding of interconnect metal
- Fracturing and lifting of insulator to release metal
- Most often occurs in top level metal



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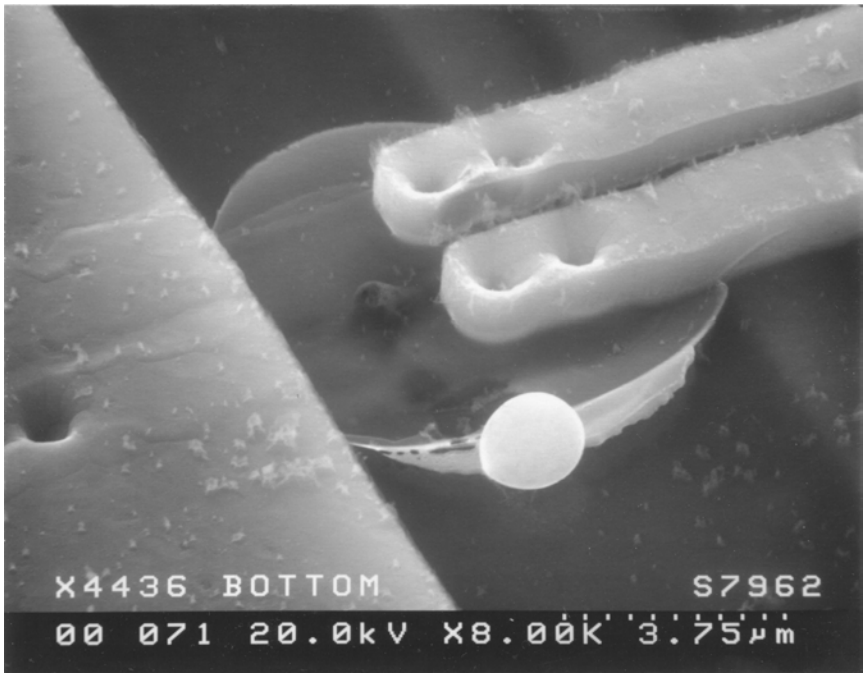
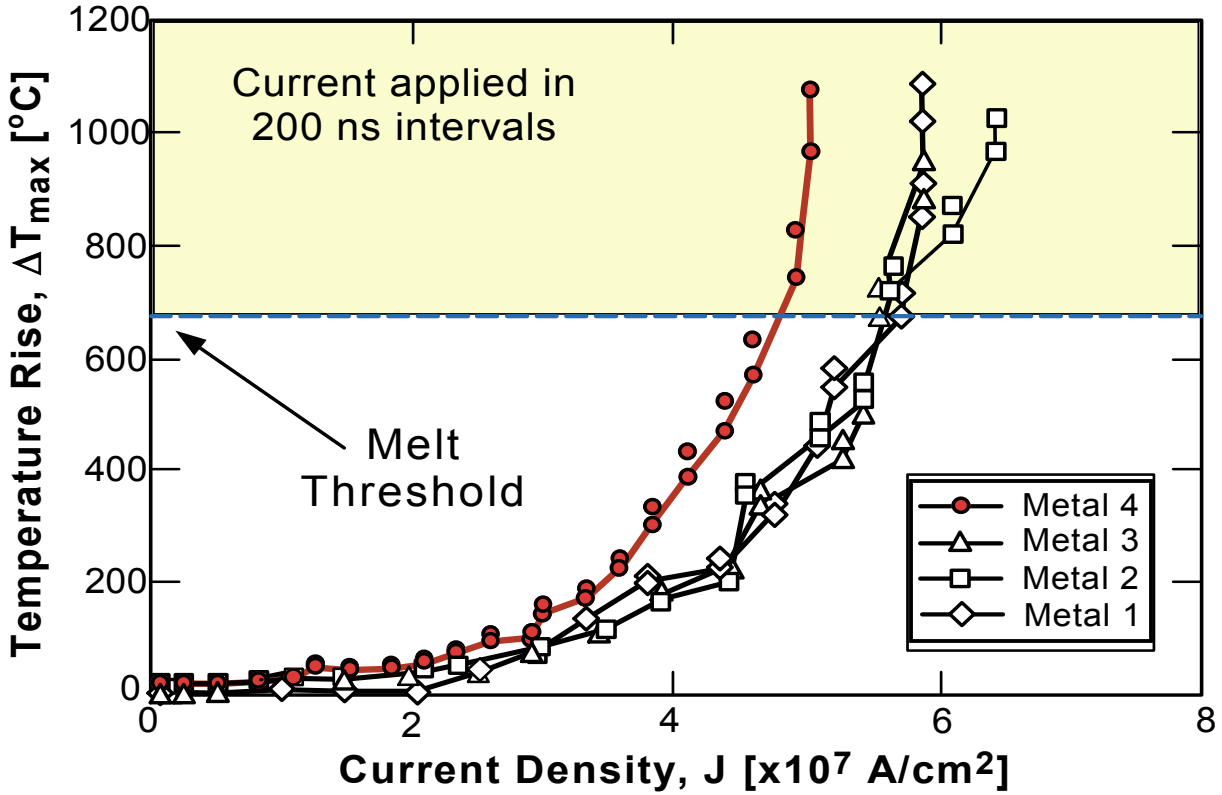


Data: Key Parameters of Latent Damage

- Minimum Current Density: 10^7A/cm^2
  - Ranged from 10^7-10^8A/cm^2
  - Based on latchup equilibrium current drawn by DUT & cross-sectional area of damaged interconnect
- Cross-sectional area of damaged interconnect: 1-10µm^2
- All tested devices of the same model were damaged in the same area on the die
  - Indicates damage is not caused by fabrication defects
- Time scale: 60µs – 18ms
- More extreme/violent than electromigration (5x10^5A/cm^2)

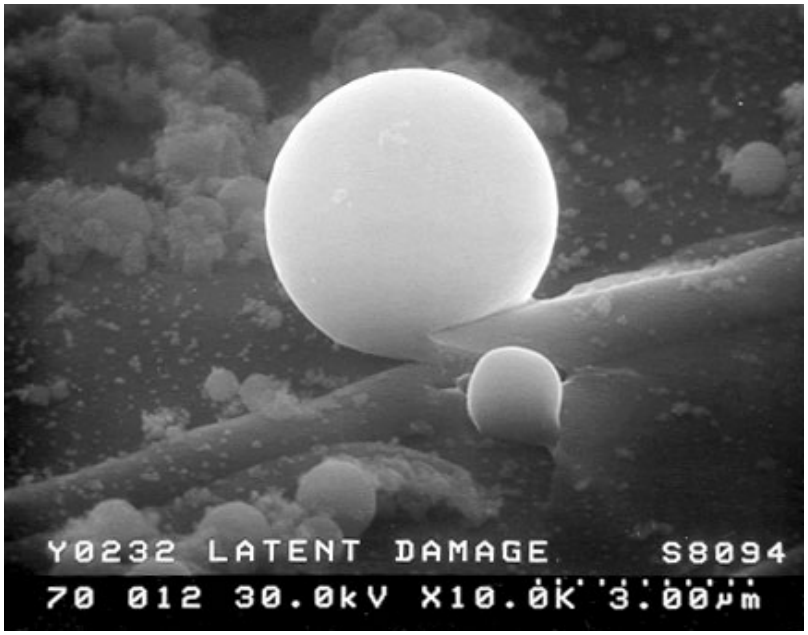
Analysis: Thermal Model



After Banerjee, et al., IEEE Elect. Dev. Lett., 18(9), 1997

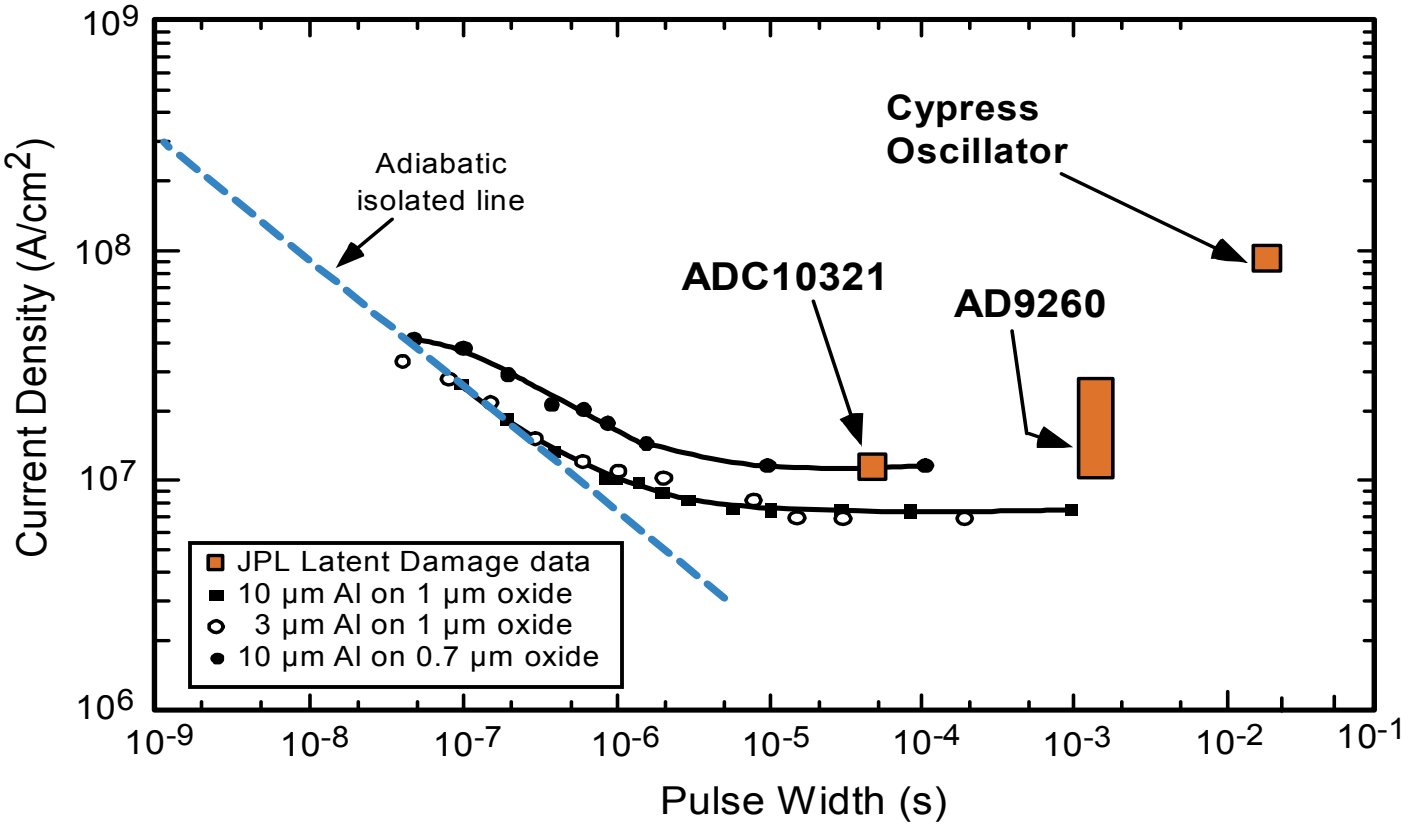
Melting & open circuit failure predicted at $5 \times 10^7 A/cm^2$ for pulses as short as 200ns

Analysis: A Physical Interpretation



- Critical current density is held long enough to melt interconnect
- Differences in thermal coefficients of expansion of metal and insulator puts mechanical stress on insulator
- Cracking of insulator and eruption of metal occur, often to the point of catastrophic voiding
- As extruded metal cools it forms most efficient spherical shape

Analysis: Latent Damage Data

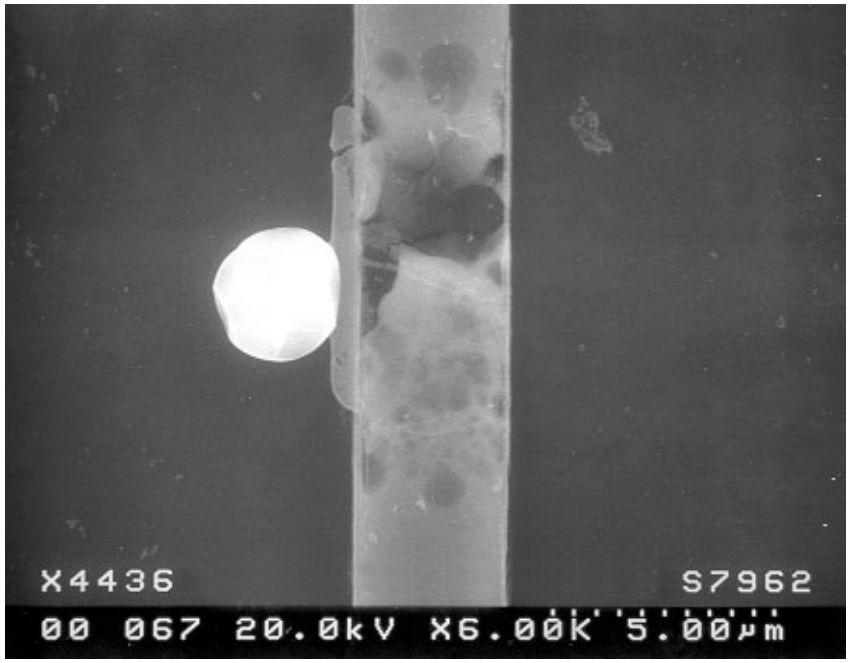


After Murguia & Bernstein, IEEE Elect. Dev. Lett., 14(10), 1993

Our data: 10^7-10^8A/cm^2 & durations of >60µs
Expect device failure, not latent damage

Analysis: Why Some Events are Not Catastrophic (Latent Damage)

- Amount of released metal may be too small to cause failure
- After melting and recrystallization, some metal may form a bridge across the void, keeping circuit closed
- Interconnect cross-section may be smaller, more susceptible to later failures



Device still *functional*

Conclusions: Impact on Future SEL Testing

- Unless you look for latent damage, you don't know it's there
- Permanent structural damage may eventually cause device failure
- Latchup circumvention should address concerns about latent damage
- The semiconductor industry is moving toward using more levels of metal and smaller interconnects

=> *next generation devices may exhibit a higher rate of latent damage*

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